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IN THE SPECIFICATION

Please add the following on page ⁶4, immediately before the header "DETAILED DESCRIPTION OF THE INVENTION":

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-- Figure 6 depicts the methodology for designing scan chains in a semiconductor chip by considering fabrication process sensitivities according to one embodiment of the invention.

Figure 7 depicts the methodology for designing scan chains in a semiconductor chip by considering fabrication process sensitivities according to a second embodiment of the invention.

Figure 8 depicts the methodology for designing scan chains in a semiconductor chip by considering fabrication process sensitivities according to a third embodiment of the invention.--

12 line 6 - page 13, line 8
Please amend the paragraph beginning on page 8, line 1 -- ~~page 8, line 23~~ as

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follows:

As now described with respect to Fig. 6 and 7, The the overall methodology of the present invention is as follows:

1. analyze specific fabrication process sensitivities of all latch cells and specific chip layer/level connectivity combinations;
2. cluster latches into scan chains using a combination of the existing location and scan length constraints, with an additional latch type constraint to maximize the latch uniformity by scan path;
3. optionally optimize step 2 to better balance scan chain content with routability, and other chip design constraints;
4. record latch type content by scan chain;
5. divide subsets of scan paths to be routed using restricted levels (this places a

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restriction only on subsets of a scan chain rather than an entire scan chain to balance routability against diagnosability);

6. assign layer subsets to these scan paths;
7. route these scan paths using restricted layer/level usage rules where possible, and relax rules where necessary to accommodate routability problems;
8. optionally optimize steps 5-7, scan path subset, and layer/level subset, based on routability analysis if needed;
9. record chip layer/level content by scan chain;
10. analyze scan chain failures for clustering by similar content, e.g. if four scan paths are failing all with a high content of metal layer/level M4;
11. correlate content back to process root cause based on the analysis in step 1 to create a list of likely root causes;
12. verify likely root cause using standard failure analysis methods.

Please amend the paragraph bridging page ¹³8 and page ¹⁴9 as follows:

As now described with respect to Fig. 8, The the process sensitive scan chain design and test methodology is as follows:

1. assemble a list of latch and chain design parameters which are sensitive to process variation or integrity, including
 - layer/level usage ==> which layer/level dominates latch (for example, considering inter-latch wiring as a design parameter, one group of latches might use inter-latch wires within dense nestings of surrounding wires, while another group might use lone inter-latch wires with nothing but fill in the neighborhood),
 - via usage,
 - location on chip,
 - scan length, including the latch count and the wire length,
 - critical area,
 - redundant vs. non-redundant elements (i.e. vias),
 - voltage domain,
 - clock domain distribution, and

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